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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/672,345	09/28/2000	David I. Poisner	10559/364001/P8247-2	7729	
20985 75	590 04/08/2003				
FISH & RICHARDSON, PC			EXAMINER		
4350 LA JOLLA VILLAGE DRIVE SUITE 500			KIM, HONG CHONG		
SAN DIEGO, O	CA 92122		ART UNIT	PAPER NUMBER	
			2186	19	
			DATE MAILED: 04/08/2003	17	

Please find below and/or attached an Office communication concerning this application or proceeding.

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i		Application No.	Applicant(s)			
Office Action Summary		09/672,345	POISNER, DAVID I.			
		Examiner	Art Unit			
		Hong C Kim	2186			
The MAILING DATE Period for Reply	of this communication ap	pears on the cover sheet w	ith the correspondence address			
after SIX (6) MONTHS from the ma - If the period for reply specified about - If NO period for reply is specified a - Failure to reply within the set or ex	FHIS COMMUNICATION. le under the provisions of 37 CFR 1. ailing date of this communication. to less than thirty (30) days, a rep bove, the maximum statutory period tended period for reply will, by statut ter than three months after the mailin	136(a). In no event, however, may a	reply be timely filed ty (30) days will be considered timely. NTHS from the mailing date of this communic BANDONED (35 U.S.C. § 133).	cation.		
1) Responsive to com	munication(s) filed on 24	<u>March 2003</u> .				
2a) This action is FINA	L. 2b)⊠ T	his action is non-final.				
		vance except for formal ma r Ex parte Quayle, 1935 C.	tters, prosecution as to the mer D. 11, 453 O.G. 213.	rits is		
4)⊠ Claim(s) <u>1-30</u> is/are	nending in the application	'n				
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5) Claim(s) is/ar						
6)⊠ Claim(s) <u>1-30</u> is/are						
7) Claim(s) is/ar	-					
8) Claim(s) are	subject to restriction and/	or election requirement.				
Application Papers						
9) The specification is o	bjected to by the Examine	er.				
10)☐ The drawing(s) filed o	on is/are: a)□ acce	epted or b) objected to by t	the Examiner.			
		ne drawing(s) be held in abey	• •			
			disapproved by the Examiner.			
	d drawings are required in re	• •				
12) The oath or declaration		xaminer.	· .			
Priority under 35 U.S.C. §§ 1						
13) Acknowledgment is	_	In priority under 35 U.S.C.	§ 119(a)-(d) or (f).			
a) ☐ All b) ☐ Some *	•—		,			
<u></u>	es of the priority documen					
		ts have been received in A				
application	າ from the International Bເ	ority documents have been ureau (PCT Rule 17.2(a)). t of the certified copies not	received in this National Stage received.	<del>}</del>		
14) Acknowledgment is m	14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).					
a) ☐ The translation of 15)☐ Acknowledgment is m		ovisional application has b				
Attachment(s)						
Notice of References Cited (PT 2)  Notice of Draftsperson's Patent 3) Information Disclosure Statement	Drawing Review (PTO-948)	5) Notice of	Summary (PTO-413) Paper No(s) Informal Patent Application (PTO-152)			

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#### **Detailed Action**

- 1. Claims 1-30 are presented for examination. Claims 31-33 has been canceled by the amendment. This office action is in response to the RCE filed on 3/24/03.
- 2. Receipt is acknowledged of information disclosure statement filed on 1/12/01, which the statement has been placed of record in the file. Information disclosed and listed on PTO 1449 was considered.

# Claim Rejections - 35 USC § 112

3. Claims 1-30 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It appears that routing a data access from a peripheral device to a first main memory in the computer and not to a second multiported memory in the computer and routing a status access from the peripheral device to the second multi-ported memory in the computer and not to the first main memory in the computer was not described in the specification at the time the application was filed.

### Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

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basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 5. Claims 1-6 and 9-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Dinwiddie, Jr. et al. (Dinwiddie) US Patent 4,371,932.

As to claim 1, Dinwiddie discloses the invention as claimed. Dinwiddie discloses a computer system, comprising: a noncached multi-ported memory (Fig. 1 Ref. 25, 27, and 30, bidrectional arrows on both sides reads on this limitation, col. 14 lines 60-63); a main memory (Fig. 1 Ref 7 or 22 or 15), a CPU coupled to the multi-ported memory (Fig. 1 Ref. 25 or 29); a bus (Fig. 1 Ref. 16) configured to communicate with one or more peripheral devices (Fig. 1 Refs. 3, 4, 5 & 6) coupled to the multi-ported memory and configured to access the multiported memory independently of the CPU; wherein the computer system is configured so that control accesses from the CPU are directed to the multiported memory and not to the main memory (Fig. 1 addr bus & command register, Ref. 25 and col. 14 lines 47-63) and data accesses from the CPU are directed to the dual-ported memory (Col. 5 lines 9-10 and 48-49).

As to claim 27, Dinwiddie discloses the invention as claimed above. Dinwiddie integrated circuit comprising a memory controller including at least two electrical ports for coupling to communication channel (Fig. 1)

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As to claim 2, Dinwiddie discloses the invention as claimed above. Dinwiddie further discloses an OS is configured such that accesses to the multiported are not cached (Fig. 1).

As to claims 3 and 27, Dinwiddie discloses the invention as claimed. Dinwiddie further discloses the multi-ported memory is dual ported (Fig. 1 Ref. 25).

As to claim 4, Dinwiddie discloses the invention as claimed above. Dinwiddie further discloses the multiported memory is embedded within a memory controller (Fig. 1).

As to claim 5, Dinwiddie discloses the invention as claimed above. Dinwiddie further discloses the multiported memory and memory controller are integrated into a single chip (Fig. 1).

As to claims 6 and 29, Dinwiddie discloses the invention as claimed above. Dinwiddie further discloses SRAM (col. 14 line 60, register read on this limitation).

As to claim 9, Dinwiddie discloses the invention as claimed above. Dinwiddie further discloses I/O bus (Fig. 1 Ref. 16).

As to claim 10, Dinwiddie discloses a method comprising: routing a data access from a

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peripheral device to a first memory in the computer and not to a second memory in the computer (Fig. 1 Ref. 7 or 22 or 15) and routing a status access from the peripheral device to the second memory in the computer and not to the first memory in the computer (Fig. 1 Ref. 25 or 30).

As to claim 11, Dinwiddie further discloses main memory (Fig. 1 Ref. 7 or 22 or 15).

As to claim 12, Dinwiddie discloses the invention as claimed above. Dinwiddie further discloses the second memory comprises memory included in a memory controller (Fig. 1 Ref 2).

As to claim 13, Dinwiddie further discloses dual ported (Fig. 1 Ref. 25 and col. 14 lines 47-63).

As to claims 14 and 16-18, claims 14, and 16-18 are a rephrasing of claims 10-13 in a computer software form. The claims are rejected for the same reason as set forth above in claims

As to claim 15, Dinwiddie further discloses I/O controller (Fig. 1 Ref. 2).

As to claim 19, Dinwiddie discloses a method comprising: routing a data access from a CPU to a first memory in the computer and not to a second memory in the computer (Fig. 1 Ref. 7 or 22 or 15) and routing a control access from the CPU to the second memory in the computer

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and not to the first memory in the computer (Fig. 1 Ref. 25 or 30).

As to claim 20, Dinwiddie further discloses main memory (Fig. 1 Ref. 7 or 22 or 15).

As to claim 21, Dinwiddie further discloses the second memory comprises memory included in a memory controller (Fig. 1 Ref 2).

As to claim 22, Dinwiddie further discloses dual ported (Fig. 1 Ref. 25 and col. 14 lines 60-63).

As to claims 23-26, claims 23-26 are a rephrasing of claims 19-22 in a computer software form. The claims are rejected for the same reason as set forth above in claims 19-22

## Claim Rejections - 35 USC § 103

- 6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 7. Claims 7 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over

  <u>Dinwiddie, Jr. et al. (Dinwiddie) US Patent 4,371,932</u> in view of <u>McMahon et al (McMahon) US</u>

#### Patent 5,784,699.

As to claims 7 and 30, Dinwiddie discloses the invention as claimed above. However, Dinwiddie does not specifically disclose reservation bits mapped to block of general purpose memory in the multiported memory. McMahon discloses reservation bits mapped to block of general purpose memory in the multiported memory (Fig. 3A) for the purpose of providing fast search and allocation/dealloction of availability of a block (col. 3 lines 7-26).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate reservation bits mapped to block of general purpose memory in the multiported memory as shown in McMahon into the invention of Dinwiddie because it would provide fast search and allocation/dealloction of availability of a block.

- 8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Dinwiddie</u>, <u>Jr. et al. (Dinwiddie) US Patent 4,371,932</u> in view of <u>Young et al (Young) US Patent 5,546,554</u>.

As to claim 8, Dinwiddie discloses the invention as claimed above. However, neither

Dinwiddie does not specifically disclose virtual addresses within multiported are mapped to

physical address with smart addressing. Young discloses virtual addresses within multiported are

mapped to physical address with smart addressing (Fig. 5a) for the purpose of memory that appears to an application to be larger and more uniform than it is.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate virtual addresses within multiported are mapped to physical address with smart addressing as shown in Young into the invention of Dinwiddie because it would provide capability of memory that appears to an application to be larger and more uniform than it is.

### Response to Amendment

10. Applicant's arguments filed on 3/24/03 have been fully considered but they are not persuasive.

Applicant's argument that the reference does not disclose routing a data access from a peripheral device to a first main memory in the computer and not to a second multiported memory in the computer and routing a status access from the peripheral device to the second multi-ported memory in the computer and not to the first main memory in the computer is not considered persuasive. Dinwiddie discloses routing a data access from a peripheral device to a first main memory in the computer and not to a second multiported memory in the computer (Fig. 1 Ref. 22 or 15 or 7) and routing a status access from the peripheral device to the second multi-ported memory in the computer and not to the first main memory in the computer (Fig. 1 Ref. 25 or 30).

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### Conclusion

- 11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
- 12. a shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).
- 13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).
- 14. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.
- 15. Any inquiry concerning this communication or earlier communications from the

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Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

## 16. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks Washington, D.C. 20231

#### or faxed to TC-2100:

After-Final

(703) 746-7238

Official

(703) 746-7239 (for formal communications intended for

entry)

Non-Official/Draft (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK

Primary Patent Examiner

April 7, 2003

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